PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Edward Y. CHANG et. al.
Serial No: 10/699,839
Filed: November 4, 2003
Atty Dkt: CHAN3228/EM

For: Growth of GaAs Epitaxial Layers On Si Substrate By Using A Novel GeSi Buffer Layer

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to Rule 37 C.F.R. §1.51(b), §1.56, §1.97, and §1.98, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper.

This Information Disclosure Statement is submitted prior to the mailing date of the first Office Action on the merits received by Applicant in the above identified application.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 02-0200.

Respectfully submitted,

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Date: March 31, 2004

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B/O Form PTO-1449	Atty. Docket Number	Serial Number
U.S. Department of Commerce Patent and Trademark Office	CHAN3228/EM	10/699,839
	Applicant Edward Y. CHANG et. al.	
Information Disclosure Statement by Applicant	Filing Date November 4, 2003	Group Unassigned

U.S. Patent Documents

Examiner Initial		Document Number	Date	Patentee/Applicant	Class	Subclass	Filing Date if Appropriate
		5,959,308	09/28/1999	Shichijo et. al.			01/29/1993
		5,879,962	03/09/1999	DePuydt et. al.			12/13/1995
		5,473,174	12/05/1995	Ohsawa			11/28/1994
		5,308,444	05/03/1994	Fitzgerald, Jr. et. al.			05/28/1993
		5,438,951	08/08/1995	Tachikawa et. al.			12/20/1993
		5,238,869	08/24/1993	Shichijo et. al.			07/27/1992
		5,183,776	02/02/1993	Lee			08/03/1989
		5,141,893	08/25/1992	Ito et. al.			02/20/1991
		6,291,321	09/18/2001	Fitzgerald			03/09/1999
		6,107,635	08/22/2000	Palathingal			06/11/1998

Foreign Patent Documents

Examiner Initial		Document Number	Publication Date	Country/Agency	Class	Subclass	Translation	
							Yes	No

Other Documents (Including Author, Title, Date, Pertinent Pages, Place of Publication, Etc.)

		J. A. Carlin et. al., *Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates*, April 2000, American Institute of Physics, Applied Physics Letters, Vol. 76, No. 14, pp. 1884-1886.
		R. D. Bringans et. al., *Use of ZnSe as an interlayer for GaAs growth on Si*, July 1992, American Institute of Physics, Applied Physics Letters, Vol. 61, No. 2, pp. 195-197.
		J. Arokiaraj et. al., *High-quality GaAs on Si substrate by the epitaxial lift-off technique using SeS_2*, December 1999, American Institute of Physics, Applied Physics Letters, Vol. 75, No. 24, pp. 3826-3828.
		C. Kadow et. al., *Subpicosecond carrier dynamics in low-temperature grown GaAs on Si substrates*, October 1999, American Institute of Physics, Applied Physics Letters, Vol. 75, No. 17, pp. 2575-2577.
		Y. R. Xing et. al., *Growth of high quality gallium arsenide on HF-etched silicon (001) by chemical beam epitaxy*, April 1993, American Institute of Physics, Applied Physics Letters, Vol. 62, No. 14, pp. 1653-1655.
		Michael Y. Frankel et. al., *Integration of low-temperature GaAs on Si substrates*, January 1993, American Institute of Physics, Applied Physics Letters, Vol. 62, No. 3, pp. 255-257.

Examiner	Date Considered

***EXAMINER:** Initial if citation is considered, whether or no t citation is in conf ormance with MPEP 609; Dra w a line thr ough citation if not in conformance and not considered. Include copy of this form with next communication to applicant.*